WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a plurality of word lines;

first and second bit lines; and

a plurality of memory cells, each of the plurality of memory cells having first and second P-channel type MISFETs, and third, fourth, fifth, and sixth N-channel type MISFETs,

wherein drains of the first and third MISFETs are connected to gates of the second and fourth MISFETs, gates of the first and third MISFETs are connected to drains of the second and fourth MISFETs, a source-drain path of the fifth MISFET is connected between said first bit line and the drain of the third MISFET, a source-drain path of the sixth MISFET is connected between said second bit line and the drain of the fourth MISFET,

wherein regions forming channels of the first to fourth MISFETs are in a floating state, and

wherein regions forming channels of the fifth and sixth MISFETs are coupled to a first wiring line supplying a potential.

2. The semiconductor device according to claim 1, wherein said semiconductor device is a semiconductor chip, having first and second semiconductor layers, and an

insulating film provided between the first and second semiconductor layers,

wherein diffusion layers of the first to sixth MISFETs are formed in the first semiconductor layer, and

wherein regions forming channels of the first to sixth MISFETs are each separated by an insulating layer.

3. The semiconductor device according to claim 2,

wherein a potential of the region forming the channel of the fifth MISFET is controlled by a potential of a word line connected to the gate of the fifth MISFET,

a potential of the region forming the channel of the sixth MISFET is controlled by a potential of a word line connected to the gate of the sixth MISFET, and

a potential of the region forming the channels of the fifth and sixth MISFETs in a memory cell connected to a non-selected word line of the plurality of word lines is lower than the potential of the region forming the channels of the fifth and sixth MISFETs in a memory cell connected to a selected word line of the plurality of word lines.

4. The semiconductor device according to claim 2,

wherein while a word line is selected and a word line is not selected, a same potential is supplied to the first wiring line.

5. The semiconductor device, according to claim 1,

wherein said semiconductor device is a semiconductor chip having first and second semiconductor layers and an insulating layer in between the first and second semiconductor layers,

wherein a voltage larger than an operating voltage applied to the memory cell is applied to the second semiconductor layer,

wherein diffusion layers of the third to sixth MISFETs are formed in the first semiconductor layer, and

wherein the first and second MISFETs are vertical MISFETs, each of which has a source region, a channel region, and a drain region deposited above the first semiconductor layer.

6. A semiconductor device, comprising:

a memory cell having first and second load P-channel type MISFETs, first and second driver N-channel type MISFETs, and first and second transfer N-channel type MISFETs,

wherein gate and channel regions of the first transfer N-channel type MISFET is coupled to each another,

wherein gate and channel regions of the second transfer N-channel type MISFET are coupled to each another,

wherein gate and channel regions of the first load P-channel type MISFET are not coupled to each another,

wherein gate and channel regions of the second load P-channel type MISFET are not coupled to each another,

wherein gate and channel regions of the first driver N-channel type MISFET are not coupled to each another, and wherein gate and channel regions of the second driver N-channel type MISFET is not coupled to each another.

7. The semiconductor device according to claim 6, further comprising:

a plurality of word lines;

a plurality of bit lines; and

a plurality of said memory cells,

wherein a potential of the channel region of the first transfer N-channel type MISFET in a memory cell connected to the non-selected word line of the plurality of word lines is lower than a potential of the channel region of the first transfer N-channel type MISFET in the memory cell connected to a selected word line of the plurality of word lines, and

wherein said plurality of memory cells are formed on a SOI substrate.

8. The semiconductor device according to claim 7,

wherein a voltage larger than an operating voltage

of the memory cells is applied to the SOI substrate, and

wherein the channel regions of the first and second driver N-channel type MISFETs and the first and second transfer N-channel type MISFETs are separated by insulating layers.

9. A semiconductor device, comprising:

a first semiconductor layer;

a second semiconductor layer; and

an insulating layer between the first and second semiconductor layers,

wherein diffusion layers of a plurality of first MISFETs are formed in the first semiconductor layer,

wherein a portion of said second semiconductor layer has a first semiconductor region, where said first semiconductor layer and said insulating layer are not covered,

wherein a supply region, which is of the same conductivity type and has a larger impurity density than said first semiconductor region, is formed in said first semiconductor region, and

wherein the threshold voltages of the plurality of first MISFETs are made to vary by supplying a voltage to the supply region.

10. The semiconductor device according to the clam 9,

wherein the supply region is formed in the shape of a ring surrounding a region covered with the first semiconductor layer and the insulating layer,

wherein in first semiconductor region the supply region and the second semiconductor region, which forms a PN junction with the second semiconductor layer, are formed,

wherein in the second semiconductor region a third semiconductor region, which forms a PN junction with the second semiconductor region, is formed,

wherein in the second semiconductor region a plurality of second MISFETs, in which their diffusion layers forms a PN junction with the second semiconductor region, are formed, and

wherein in the third semiconductor region a plurality of third MISFETs, in which their diffusion layers forms a PN junction with the third semiconductor region, are formed.

11. The semiconductor device according to claim 10,

wherein gate insulating films of the plurality of first and second MISFETs are formed by the same steps.

12. The semiconductor device according to claim 10,

wherein the second semiconductor layer is N-type, and

wherein a voltage applied to the supply region is higher than an operating voltage of the plurality of first MISFETs.

13. The semiconductor device according to claim 10,

wherein the first semiconductor layer includes a static memory cell, and

wherein the second and third semiconductor regions include I/O circuits.

14. The semiconductor device according to claim 13,

wherein a logic circuit is further formed in the first semiconductor layer, and

wherein a switch circuit for controlling an operating voltage of the logic circuit and an analog circuit are further formed in the second and third semiconductor regions.

15. A semiconductor device, formed on a semiconductor chip, comprising:

a first circuit portion including a plurality of first MISFETs of a first conductivity type and a plurality of second MISFETs of second conductivity type; and

a second circuit portion including a plurality of

third MISFETs,

wherein the semiconductor chip includes a first conductivity type semiconductor substrate with an insulating layer embedded therein,

wherein the semiconductor substrate includes a first semiconductor region forming a PN junction with the semiconductor substrate, and a second semiconductor region of a second conductive type having a higher impurity density than an impurity density of the semiconductor substrate,

wherein the first semiconductor region includes a third semiconductor region forming a PN junction the semiconductor substrate,

wherein a semiconductor region on the insulating layer includes diffusion layers of the plurality of third MISFETs,

wherein diffusion layers of the plurality of first MISFETs form a PN junction with the first semiconductor region,

wherein diffusion layers of the plurality of second MISFETs form a PN junction with the third semiconductor region, and

wherein a first voltage is applied to the second semiconductor region.

16. The semiconductor device according to claim 15,

wherein the first conductivity type is of N-type and the first voltage is higher than the operating voltage applied to the second circuit portion.

17. The semiconductor device according to claim 16,

wherein the second circuit portion includes a static type memory cell, and

wherein the first circuit portion includes an I/O circuit.

18. The semiconductor device according to claim 17,

wherein the second circuit portion further includes a logic circuit, and

wherein the first circuit portion further includes a switch circuit for controlling the operating voltage of the logic circuit.

19. The semiconductor device according to claim 18,

wherein gate electrodes of the plurality of third MISFETs are made of silicon germanium, and

wherein P-type dopants are implanted to gate electrodes of the plurality of third MISFETs of both P-channel and N-channel type.

20. The semiconductor device according to claim 17,

wherein the semiconductor substrate is formed by bonding silicon substrates together, having an insulating film therebetween, and

wherein the first to fourth semiconductor regions are formed in a portion of the bonded silicon substrate, where the silicon layer on the insulating film and the insulating film itself are removed by etching.

21. The semiconductor device according to claim 17,

wherein gate insulating films of the first to third MISFETs are formed by the same process.

22. The semiconductor device according to claim 16, further comprising:

a voltage step-down circuit made of the first and second MISFETs,

wherein the first voltage is supplied externally from a semiconductor chip,

wherein the first voltage is inputted to the voltage step-down circuit, and the operating voltage of the second circuit portion is an output from the voltage step-down circuit.

23. A semiconductor device, formed on a semiconductor substrate including a bulk portion and a SOI portion,

comprising:

a logic circuit;

a switch circuit for a controlling operating voltage applied to the logic circuit; and

an I/O circuit,

wherein the switch circuit and the I/O circuit are formed in the bulk portion, and

wherein the logic circuit is formed in the SOI portion.

24. The semiconductor device according to claim 23, further comprising:

a SRAM memory cell; and a power circuit for generating the operating voltage of the SRAM memory cell,

wherein the memory cell is formed in the SOI portion, and

wherein the power circuit is formed in the bulk portion.

25. The semiconductor device according to claim 24,

wherein gate electrodes of MISFETs of P-type and N-conductivity type channels, of which diffusion layers are formed in the SOI portion, are made of silicon germanium and P-type dopants are implanted, and

wherein a substrate potential of the SOI portion is

applied through a power supply region formed in the bulk portion.

26. A semiconductor device formed on a substrate including a first semiconductor layer, a second semiconductor, and an insulating film provided between the first and second semiconductors, comprising:

a logic circuit including a plurality of N-channel type first MISFETs and a plurality of P-channel type second MISFETs, and

a memory cell including N-channel type third, fourth, fifth, and sixth MISFETs and P-channel type seventh and eighth MISFETs,

wherein each of diffusion layers of the first to eight MISFETs is formed in the first semiconductor layer,

wherein gate electrodes of the first to eight MISFETs are made of silicon germanium, and are implanted by P-type dopants, and

wherein a voltage is applied to the second semiconductor layer.

27. The semiconductor device according to claim 26,

wherein the logic circuit has a word driver circuit driving a word line, and a sense amplifier circuit coupled to a pair of bit lines,

wherein gates of the third and four MISFETs are coupled to the word line,

wherein gates of the fifth and seventh MISFETs are coupled to drains of the sixth and eighth MISFETs,

wherein gates of the sixth and eighth MISFETs are coupled to drains of the fifth and seventh MISFETs, and

wherein potentials of channel regions of the third and fourth MISFETs vary by a potential of the word line.

28. The semiconductor device according to claim 26,

wherein a voltage higher than an operating voltage of the memory cell.

29. The semiconductor device according to claim 26,

wherein a portion of the second semiconductor layer includes a first region, in which the insulating film and the first semiconductor layer are not formed ,

wherein the first region includes an I/O circuit for inputting and outputting data externally from said semiconductor device.

30. The semiconductor device according to claim 28,

wherein a portion of the second semiconductor layer includes a first region, where the insulating film and the first semiconductor layer are not formed,

wherein the second semiconductor layer is of N-type, and

wherein a voltage is applied to the second semiconductor layer is applied through a power supply region formed in the first region.

31. The semiconductor device according to claim 30,

wherein a power circuit for generating an operating voltage of memory cells is further formed in the first region, and

wherein the power circuit has a function of dropping voltage inputted externally of the semiconductor device.

32. A semiconductor device, which includes a first semiconductor layer, a second semiconductor layer, and an insulating film between the first and second semiconductor layers, comprising:

a logic circuit including a plurality of N-channel type first MISFETs and a plurality of P-channel type second MISFETs, and

a memory cell including an N-channel type third, fourth, fifth, and sixth MISFETs, and P-channel type seventh, and eighth MISFETs,

wherein each of diffusion layers of the first to

eighth MISFETs is formed in the first semiconductor layer,

wherein gate electrodes of the first and second MISFETs are made of silicon germanium and are implanted with P-type dopants,

wherein gate electrodes of the third to sixth MISFETs are made of polysilicon and are implanted with N-type dopants,

wherein gate electrodes of the seventh and eighth MISFETs are made of polysilicon and are implanted with P-type dopants, and

wherein a voltage is applied to the second semiconductor layer.

33. The semiconductor device according to claim 32,

wherein the logic circuit includes a word driver circuit for driving a word line, a decoder circuit, and a circuit for precharging bit lines,

wherein gates of the third and fourth MISFETs are coupled to the word line,

wherein gates of the fifth and seventh MISFETs are coupled to drains of the seventh and eighth MISFETs,

wherein gates of the sixth and eighth MISFETs are coupled to drains of the fifth and seventh MISFETs, and

wherein potentials of channel regions of the third and fourth MISFETs are controlled, and the channels regions

of the fifth to eighth MISFETs are in a floating state.

34. The semiconductor device according to claim 33, wherein a voltage higher than an operating voltage of the memory cells is applied to the second semiconductor layer.

35. The semiconductor device according to claim 34, wherein the absolute value of a threshold voltage of the seventh MISFET is larger than the absolute value of a threshold voltage of the third MISFET.

36. The semiconductor device according to claim 31, wherein the first to eighth MISFETs are enhancement type MISFETs, and

wherein the second semiconductor layer is of n-type.

37. A semiconductor device, comprising:

a plurality of word lines;

first and second bit lines; and

a plurality of memory cells,

wherein each of the plurality of memory cells having P-channel type first and second MISFETs and N-channel type third and fourth MISFETs,

wherein a source-drain path of the first MISFETs are formed between the first bit line and a drain of the third MISFET, a source-drain path of the second MISFET is formed between the second bit line and a drain of the fourth MISFET, and input and output terminals of the third and fourth MISFETs are coupled to each another,

wherein a voltage applied to a first SOI base substrate, where the first MISFET is formed, is controlled by drain voltage of the fourth MISFET, and

wherein a voltage applied to a second SOI base substrate, where the second MISFET is formed, is controlled by drain voltage of the third MISFET.

38. The semiconductor device according to claim 37,

wherein the third and fourth MISFETs of the plurality of memory cells are formed on a common SOI base substrate.

39. A semiconductor device comprising:

a logic circuit; and

a switch circuit for controlling an operating voltage of the logic circuit,

wherein transistors included in the logic circuit and the switch circuit are formed on a SOI substrate,

wherein a voltage of the SOI substrate, on which the

first transistor included in the switch circuit is formed, is controlled by a signal input to a gate of the first transistor.

40. A semiconductor device, comprising:

a first power source and a second power source;

a first circuit including a plurality of first MISFETs driven by the first power source; and

a second circuit having a plurality of second MISFETs driven by the second power source,

wherein the plurality of first MISFETs and the plurality of second MISFETs are formed on a common SOI base substrate.

41. The semiconductor device according to claim 40,

wherein channel regions of the plurality of first and second MISFETs are individually controlled by two gate electrodes which are controlled by the application of a first voltage to a common SOI base substrate.